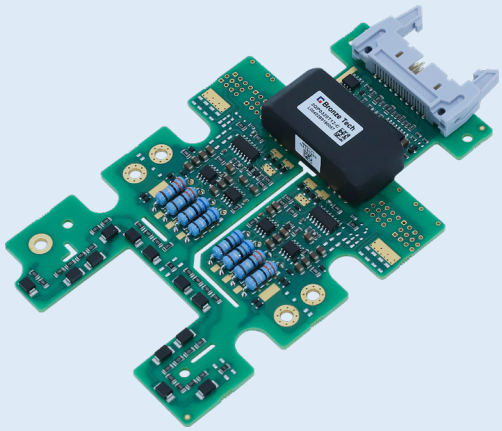
2QP0320Txx

Description & Application Manual

RoHS
COMPLIANT



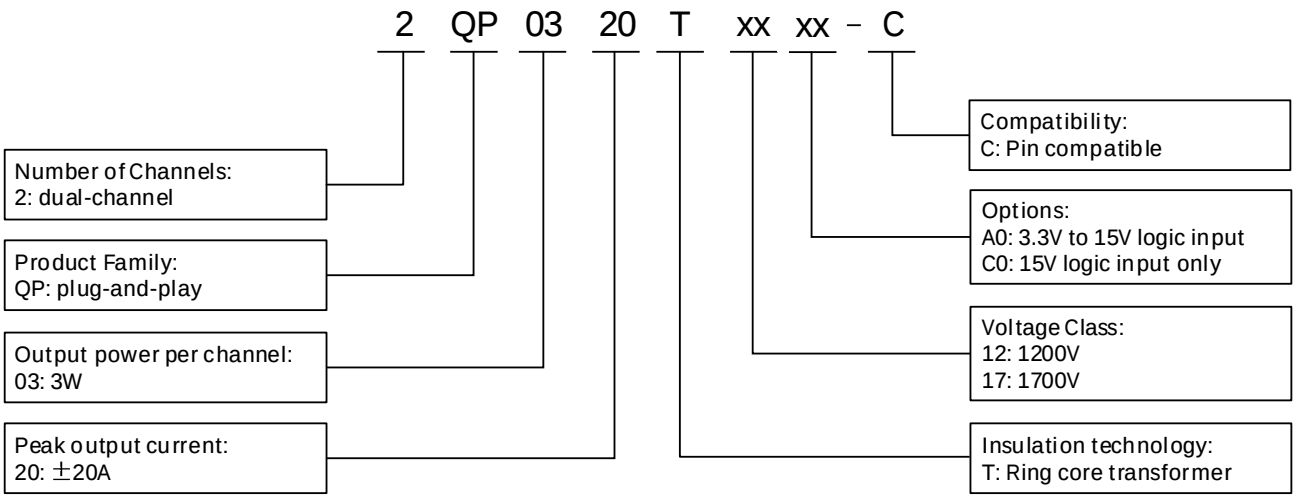
The photo is for reference only.

Description

2QP0320Txx is a medium power, dual-channel Plug-and-Play gate driver designed for high reliability applications based on the ASIC chipset developed by Bronze Technologies.
2QP0320Txx is suitable for half-bridge topology built with PrimePack™ package lGBT modules up to 1700V.
The plug-and-play capability of the driver allows immediate operation without adaptions after assembly.

Contents

Nomenclature



Block Diagram Of Driver Board

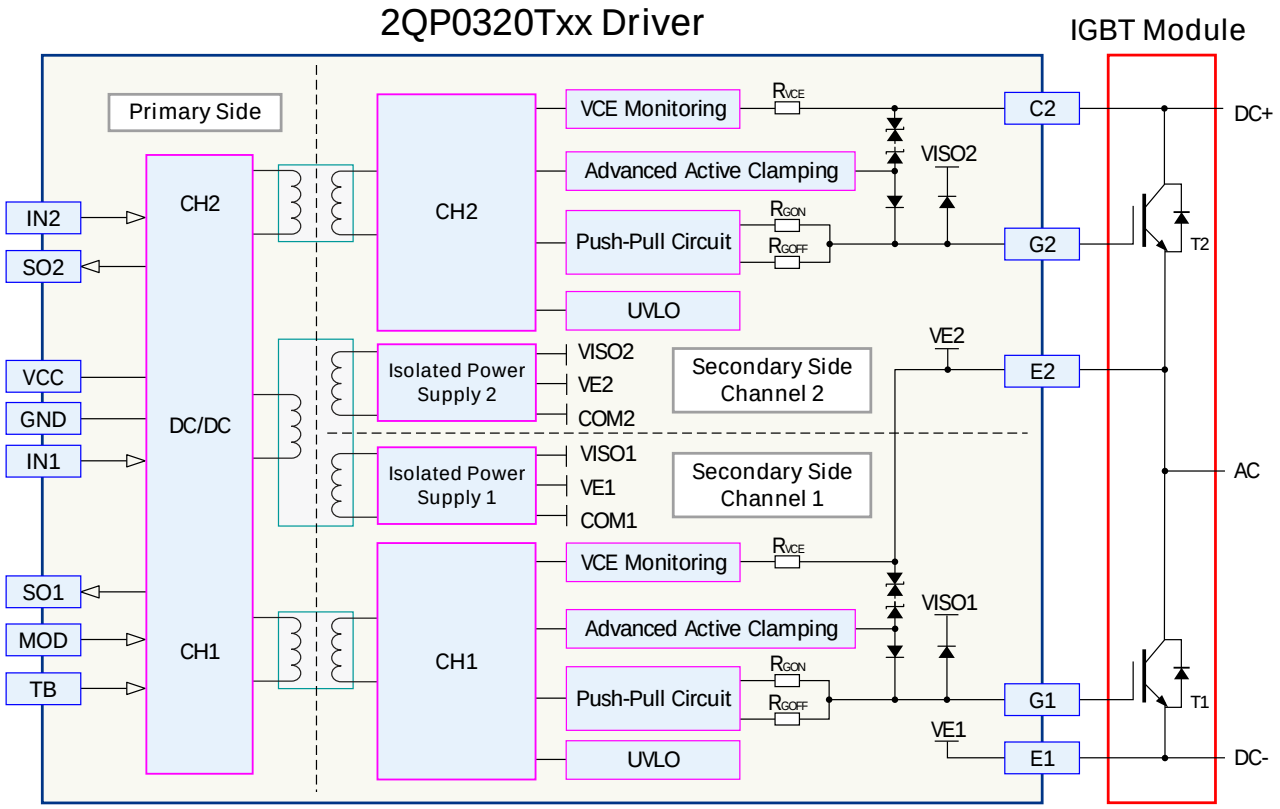


Figure 1. Block diagram of 2QP0320Txx

Recommended Interface Circuitry for Connector P1

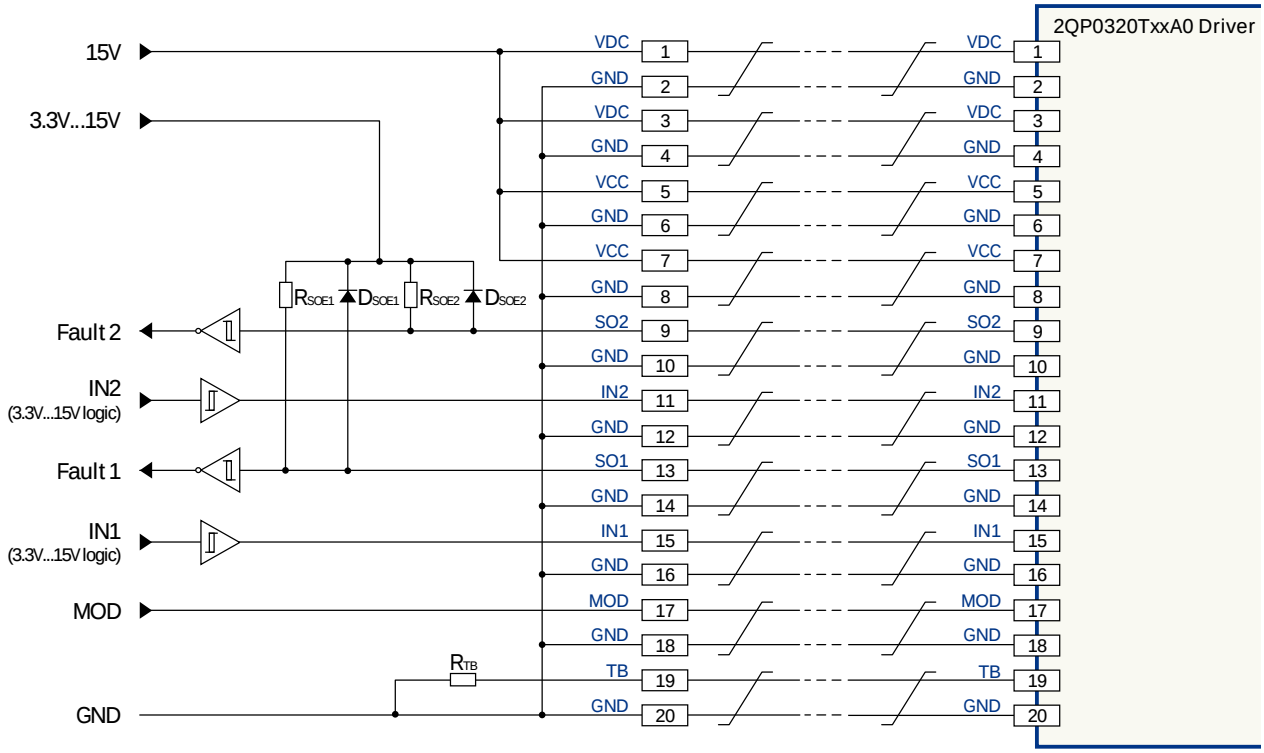


Figure 2. Recommended user interface of 2QP0320TxxA0

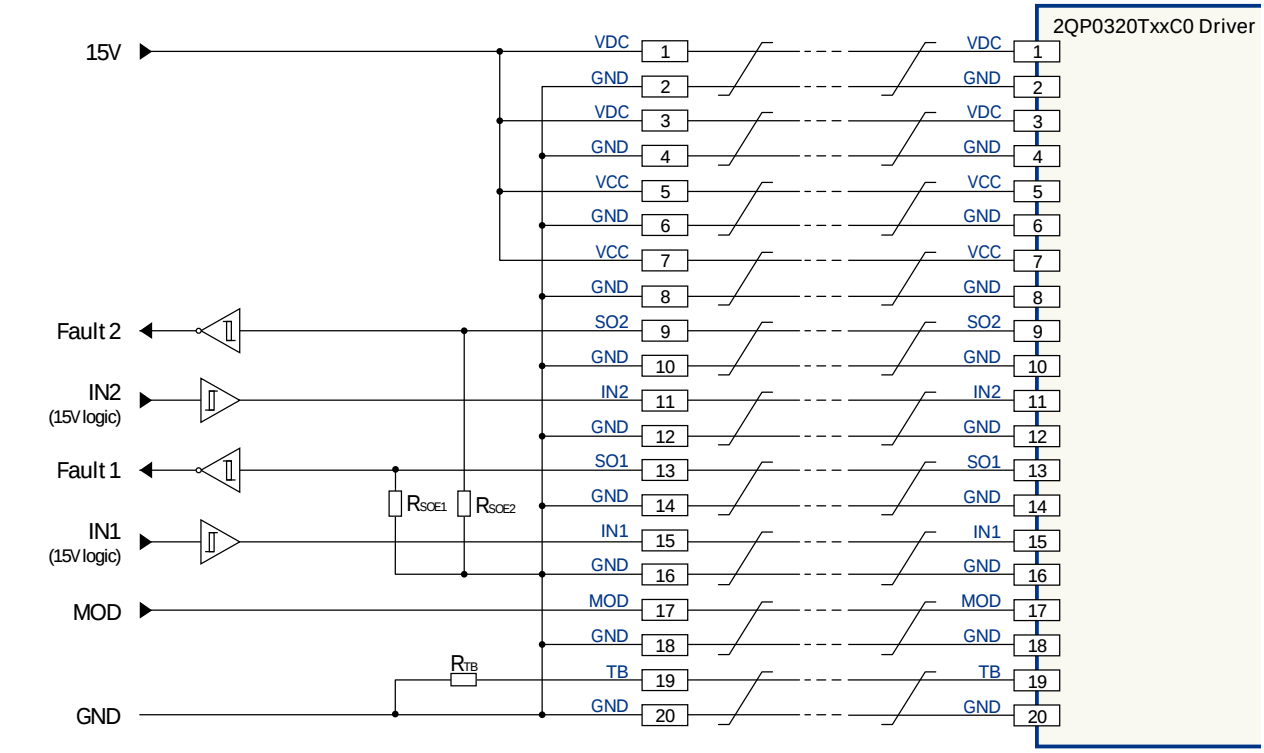


Figure 3. Recommended user interface of 2QP0320TxxC0

Direct Mode

MOD pin	IN		OUT	
	IN1	IN2	Gate1	Gate2
Left open or connected to VCC	1	1	1	1
	0	1	0	1
	1	0	1	0
	0	0	0	0

Half-bridge Mode

MOD pin	IN		OUT	
	IN1	IN2	Gate1	Gate2
Shorted to GND	1	1	1	0
	0	1	0	1
	1	0	0	0
	0	0	0	0

Block Diagram With Connection to IGBT Module

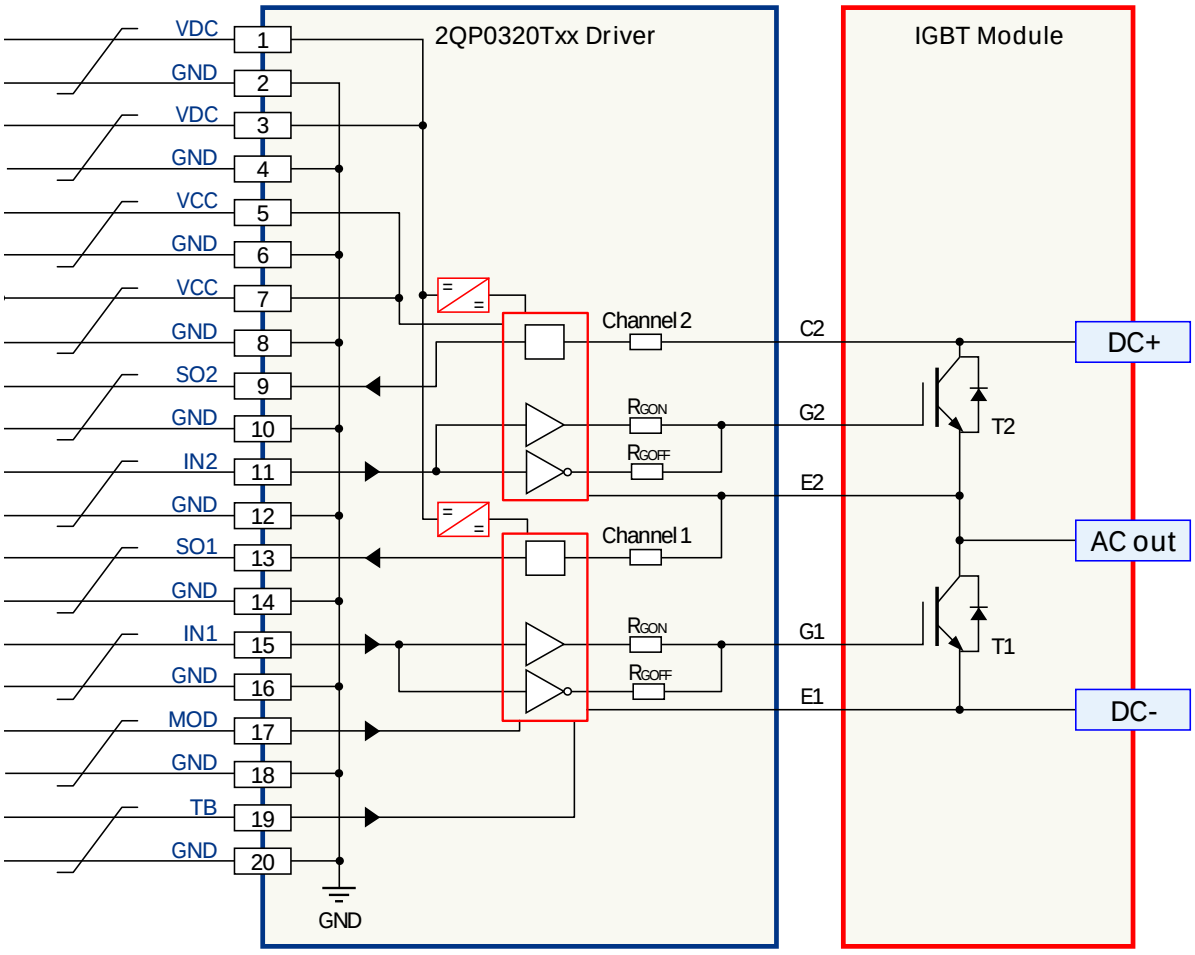


Figure 4. Block diagram covering driver 2QP0320Txx and IGBT module

Pin Designation

Connector P1[1)]

Pin	Symbol	Description	Pin	Symbol	Description
1	VDC	15V for DC/DC converter	2	GND	Ground
3	VDC	15V for DC/DC converter	4	GND	Ground
5	VCC	15V for primary side electronics	6	GND	Ground
7	VCC	15V for primary side electronics	8	GND	Ground
9	SO2	Status output channel 2	10	GND	Ground
11	IN2	Signal input channel 2	12	GND	Ground
13	SO1	Status output channel 1	14	GND	Ground
15	IN1	Signal input channel 1	16	GND	Ground
17	MOD	Mode selection (direct/half-bridge Mode)	18	GND	Ground
19	TB	Set blocking time	20	GND	Ground

Note: 1) 20-pin shrouded socket with eject hooks is default configuration.
It is recommended to use the flat cable connector 71600-020LF from FCL.

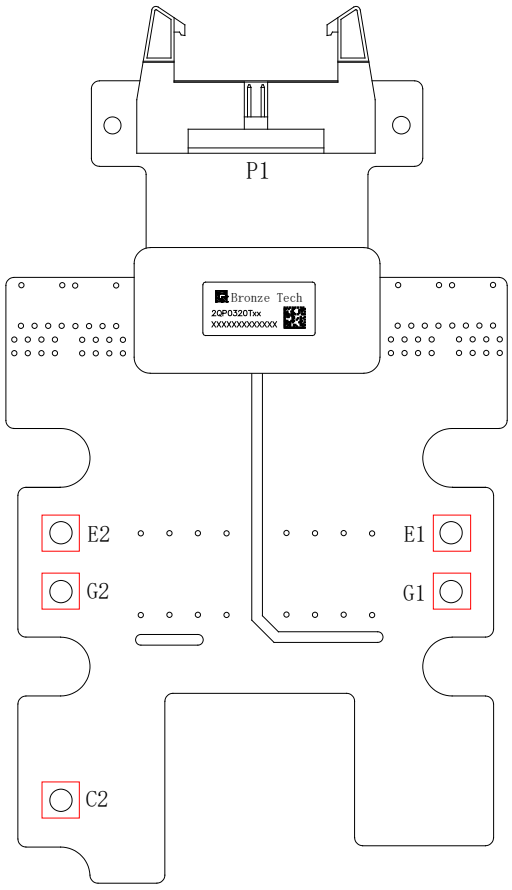


Figure 5. 2QP0320Txx Pin layout

Function Description

Power Supply and Monitoring

The DC/DC converter of the driver provides galvanic isolation between primary side power supply and secondary side gate driving circuitry.

Supply voltage monitoring is deployed for the primary-side and two secondary-sides of the DC/DC converter for undervoltage lockout (UVLO).

Note: A stable primary side supply voltage is required.

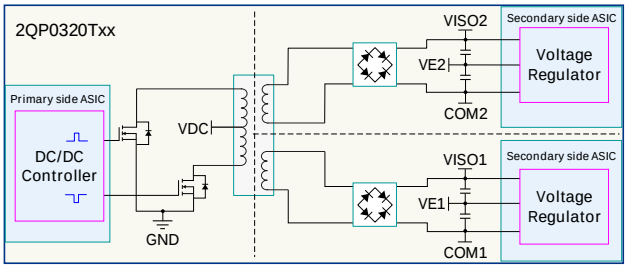


Figure 6. Power supply circuitry

Primary Side Supply Monitoring:

The supply voltage V_{CC} is monitored in the primary-side for undervoltage lockout. When V_{CC} drops to the UVLO set fault threshold V_{CCUV+}, UVLO is triggered, two secondary-side gate drive outputs are locked in off state and keep the IGBT off. Meanwhile, the fault signal SO1 and SO2 are pulled down.

When V_{CC} returns to the UVLO clear fault threshold V_{CCUVR+}, the driver continues to maintain the lockout state for a period t_B, then exits the lockout state and pulls up fault signals SOx.

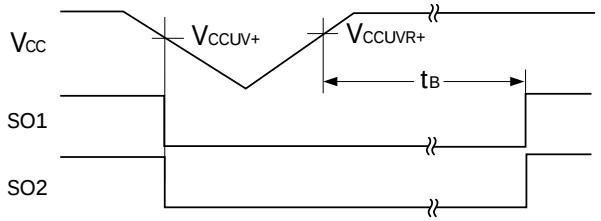


Figure 7. Primary-side UVLO logic

Secondary Side Supply Monitoring:

The secondary power supply voltage is also monitored to ensure a safe IGBT switching. To demonstrate the behavior of the secondary side UVLO, a scenario is considered in below where the primary side supply voltage V_{DC} decreases from the nominal value towards zero:

1) At first the positive voltage V+ (VISO to VE) is held constant on the nominal value, while the negative voltage V- (COM to VE) deviates from the nominal value towards zero along with the decreasing V_{CC}.

2) As soon as V- reaches -5V, V- is held constant and V+ starts to fall towards zero if V_{CC} further collapses.

3) When V+ reaches the set fault threshold V_{UV+}, UVLO protection is initiated. The IGBT is turned off and held in off state, meanwhile a set fault signal is transmitted to the primary side and asserts SOx pin immediately.

4) The counting of t_B starts when a UV fault is detected. This is different from the primary side supply voltage monitoring, where the counting of t_B starts after UV fault is cleared. If a new fault is detected before t_B of the previous fault elapses, t_B is recounted from the new fault.

5) When V_{DC} rises again, the driver firstly restores V+.

6) If V+ further increases and reaches its nominal value, V+ is held constant and V- starts to recover towards its nominal value.

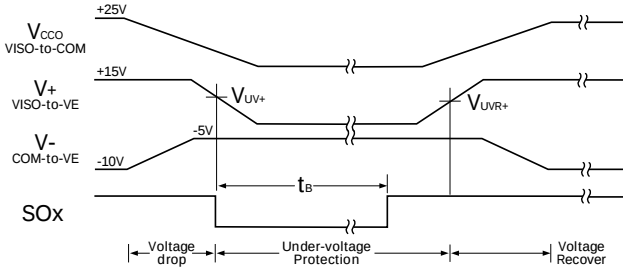


Figure 8. Secondary-side UVLO logic

Input Signal

The control signal is input from INx port. The turn-on threshold V_{INH} and turn-off threshold V_{INL} are defined by different resistor configurations on the driver board.

Part Number	R_{INx1}	R_{INx2}	R_{INx3}
2QP0320TxxA0	4.7kΩ	Unassembled	1kΩ
2QP0320TxxC0	Unassembled	1.2kΩ	3.3kΩ

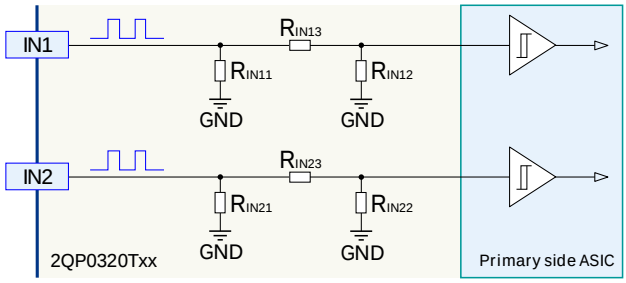


Figure 9. INx input circuitry

Transmission Logic and Mode Selection

The driver can be configured as direct or half-bridge mode. Operating mode of the driver can be configured by the MOD pin connection.

Direct Mode:

If the MOD pin is left open or connected to VCC, direct mode is selected and the two channels are independent. Input IN1 corresponds to Channel 1, while input IN2 corresponds to Channel 2. A logic high turns on the corresponding IGBT, while a logic low turns it off.

Note: In direct mode, make sure to add a proper dead time in the input signals to avoid shoot-through of the two switches in a bridge.

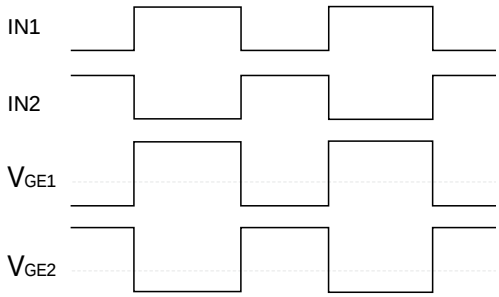


Figure 10. Transmission logic in direct mode

Half-Bridge Mode:

If the MOD pin is shorted to ground, the driver operates in half-bridge mode. In this mode, IN1 serves as PWM signal and IN2 as enabling signal.

When IN2 is low, both channels are locked in off state. If IN2 is high, both channels are enabled. The gate output signals of both channels are determined by IN1. At the transition of IN1 from low to high, the gate output of Channel 2 is turned off immediately. After a dead time DT elapses, the gate output of Channel 1 is turned on. At the transition of IN1 from high to low, the gate output of Channel 1 is turned off immediately. After the dead time DT elapses, the gate output of Channel 2 is turned on.

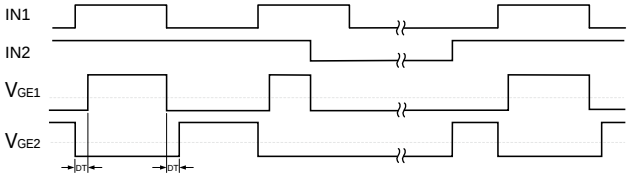


Figure 11. Transmission logic in Half-bridge mode

Status Output Signal

The output SOx has open-drain transistor on the driver board.

Part Number	R_{SOx1}	R_{SOx2}
2QP0320TxxA0-xx	33Ω	Unassembled
2QP0320TxxC0-xx	33Ω	10kΩ

2QP0320TxxA0-xx:

When there is no fault, Q_{SOx} keeps off, the SOx outputs have high impedance. An internal current source pulls the SOx outputs to a voltage of about 5V. When a fault is detected, the corresponding SOx is pulled down to ground.

It is recommended to mount external pull-up resistors as demonstrated in the diagram of SOx user interface of 2QP0320TxxA0-xx. the diodes D_{SOEx} are only required when using 3.3V input logic level. For 5V...15V logic, they can be omitted.

In a fault condition, the maximum SOx current must not exceed 20mA.

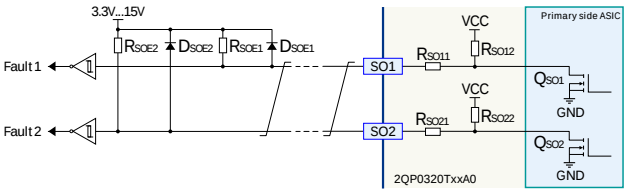


Figure 12. SOx user interface of 2QP0320TxxA0-xx

2QP0320TxxC0-xx:

When there is no fault, Q_{SOx} keeps off, and each of the SOx is pulled up to VCC via a resistor on the driver board. When a fault is detected, the corresponding SOx is pulled down to ground. It is recommended to mount external pull down resistors R_{SOEx} to ground as demonstrated in the diagram of SOx user interface of 2QP0320TxxC0-xx, which allows a missing SOx connection to be detected (safe logic in the event of a defective cable). Note that R_{SOEx} (pull down resistors on the user's board) must have sufficiently high resistance (e.g. 150 kΩ), as they form a voltage divider together with the internal pull-up resistor (typically 10kΩ) on the driver board.

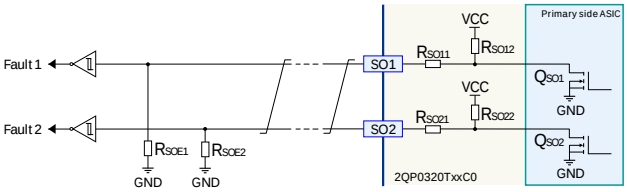


Figure 13. SOx user interface of 2QP0320TxxC0-xx

SO1 and SO2 can be connected together to provide fault information of the entire driver. However, for fast and precise fault diagnosis, it is recommended to detect the information independently.

Blocking Time Setting

The blocking time t_B can be configured by an external resistor R_{TB} between TB pin and GND.

The following formula describes the relationship between t_B and R_{TB} (at typical values).

$$R_{TB}[ms]=\frac{8250+150\cdot t_B[ms]}{95-t_B[ms]}$$

$$R_{TB} \geqslant 150k\Omega,\ 20ms \leqslant t_B \leqslant 95ms$$

When R_{TB} is 150kΩ , the blocking time t_B is about 20ms. When TB is left open, the blocking time is 95ms.

Note: R_{TB} should not be smaller than 150kΩ, which means the blocking time t_B cannot be shorter than 20ms, otherwise the blocking time t_B will be inaccurate and unstable. If TB pin is shorted to ground, t_B is fixed to 10us.

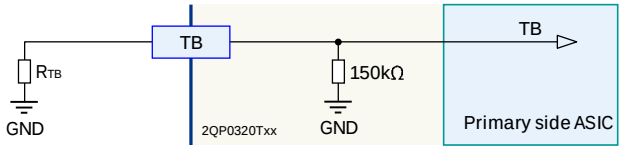


Figure 14. Blocking time setting

IGBT Turn-On and Turn-Off

To turn on the IGBT, Q_{ON} inside the ASIC of the driver is turned on and Q_{OFF} is turned off. The gate resistor R_{GON} is pulled up to charge the gate and the IGBT is turned on.

To turn off the IGBT, Q_{OFF} inside the ASIC of the driver is turned on and Q_{ON} is turned off. The gate resistor R_{GOFF} is pulled to COMx to discharge the gate and the IGBT is turned off.

To enhance the driving capability, two MOSFETs are connected in parallel with Q_{ON} and Q_{OFF}.

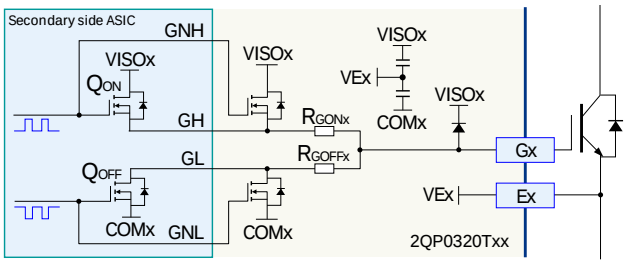


Figure 15. Gate drive output circuitry

Active Clamping

Fast IGBT turn-off may lead to voltage spikes, which is critical when DC-link voltage and load current are high. Voltage spikes can cause damage to the IGBT. The turn-off voltage spike is mainly correlated to the stray inductance Ls and the slew rate of the IGBT turn-off current di/dt.

By adjusting the turn-off gate resistor R_{GOFF}, di/dt can be reduced and the voltage overshoot is reduced. However, the impact of Ls is inevitable. It can be more pronounced under high current in short circuit or overload. The driver is equipped with active clamping function to effectively prevent the overvoltage damage on IGBT.

A feedback path from the IGBT collector to the gate is established using transient voltage suppressor devices(TVS). When the V_{CE} peak voltage exceeds the breakdown threshold, the TVS chain will break down and the current through it will charge the IGBT gate, which prolongs the IGBT in on-state but reduces the di/dt and suppresses the excessive V_{CE} of the IGBT. The break down threshold is defined as the voltage applied on the TVS chain when the leakage current becomes 1mA.

When the active clamping is activated, a current flows into the TVS chain and ACL pin on the ASIC will sense this current and the ASIC will switch off the turn-off MOSFET of the driver. Eventually it can improve the effeciveness of the active clamping and to reduce the losses in the TVS. The feature is mainly integrated in the secondary-side ASIC.

Part Number	IGBT Voltage	Typical value of TVS Chain Breakdown Threshold @25°C &I_R=1mA
2QP0320T12xx	1200V	1020V
2QP0320T17xx	1700V	1560V

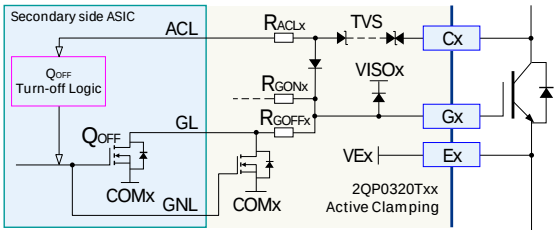


Figure 16. Active clamping circuitry

IGBT Short-Circuit Protection

The V_{CE} detection circuitry is used for IGBT short- circuit protection. The detection of two channels are independent from each other. The short-circuit detection is only valid when the IGBT is turned on. When the IGBT is in off state, the input signal turns on Q_{CEx} and clamps V_{CEDTx} to COMx. In this case, the comparator outputs logic low.

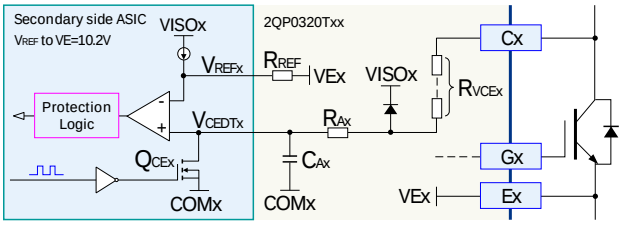


Figure 17. Short-circuit protection circuitry

Normal Turn-On:

When the logic input will turn on the IGBT, Q_{CE} is firstly turned off and releases the clamping of V_{CEDTx}. At this moment, IGBT is still in off state and V_{CE} is high. C_{Ax} is charged through the resistor chain composed of R_{VCEx} and R_{Ax}, V_{CEDTx} rises. Then the IGBT is turned on, V_{CE} quickly drops to saturation voltage V_{CE-SAT} and V_{CEDTx} reaches V_{CE-SAT}.

As V_{CE-SAT} is significantly lower than the protection threshold V_{REF}, the comparator does not flip over and the protection is not initiated.

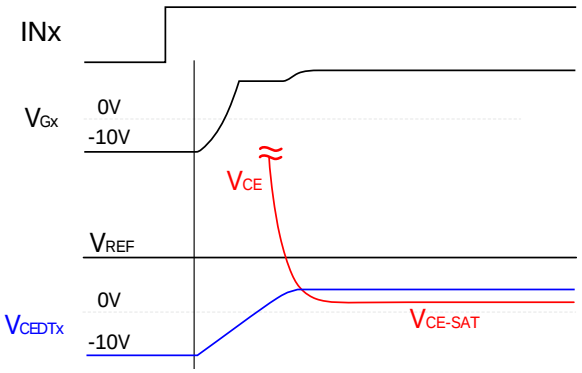


Figure 18. Signal waveform at normal turn-on

Class I Short-Circuit Protection:

When Class I short circuit (bridge shoot-through) occurs, due to the rapid increase of the short cirucit current, the IGBT desaturates and result in rapidly increased V_{CE}. C_{Ax} is charged and V_{CEDTx} rises until it is clamped at VISOx. During this process, V_{CEDTx} exceeds V_{REF} and the comparator's output flips, which consequently triggers the short-circuit protection.

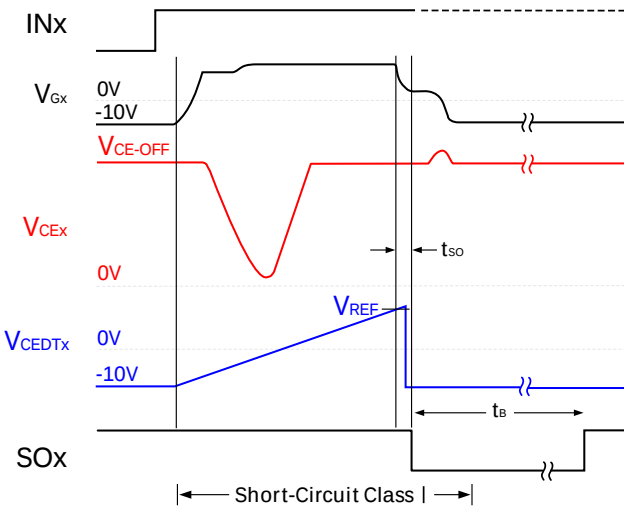


Figure 19. Class I short-circuit protection

The short-circuit protection logic turns off the IGBT immediately to ensure its safety. At the same time, set fault signal is sent to the primary side to pull down the SOx pin,so as to alert a fault state. The channel is locked in fault state for a period t_B before recovering to the normal state. The protection circuits of the two channels are independent from each other. Therefore, when short- circuit protection is initiated on one channel, the other channel remains operating normally. It is recommended to check the SOx signal timely and activate system lockout when necessary.

Class II Short-Circuit Protection:

When a Class II short circuit (e.g. phase to phase short circuit) occurs, the current ramps up slowly as the loop is relatively high. The IGBT still enters saturation state normally. As the short-circuit current increases, V_{CE} increases gradually until it exceeds the protection threshold, then the driver initiate short-circuit protection. The response time in Class II short-circuit protection is longer than that of Class I.

In another case, If bridge shoot-through occurs under low DC-link voltage, the short circuit current is low and also resulting in increased protection response time.

Note: When a Class II short circuit occurs, the short circuit impedance varies greatly, which leads to uncertain timing of IGBT desaturation. Therefore, before the protection is initiated, the IGBT may have been already damaged by a considerable sum of heat accumulated. In this case, the driver's short-circuit protection cannot guarantee the intactness of the IGBT. Extra overcurrent protection measures have to be introduced.

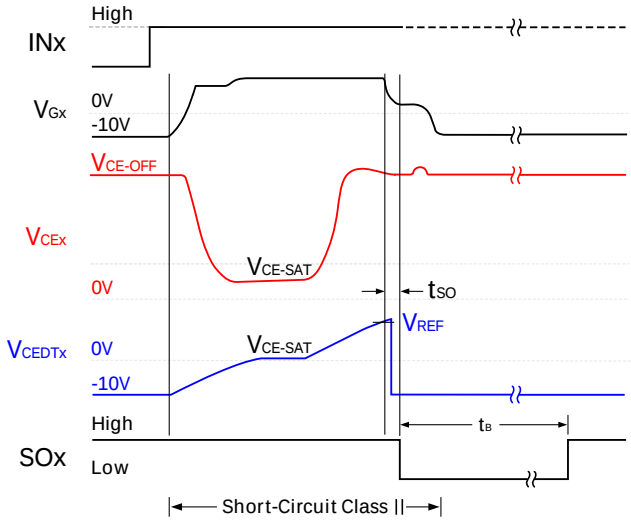


Figure 20. Class II short-circuit protection

Mechanical Dimensions

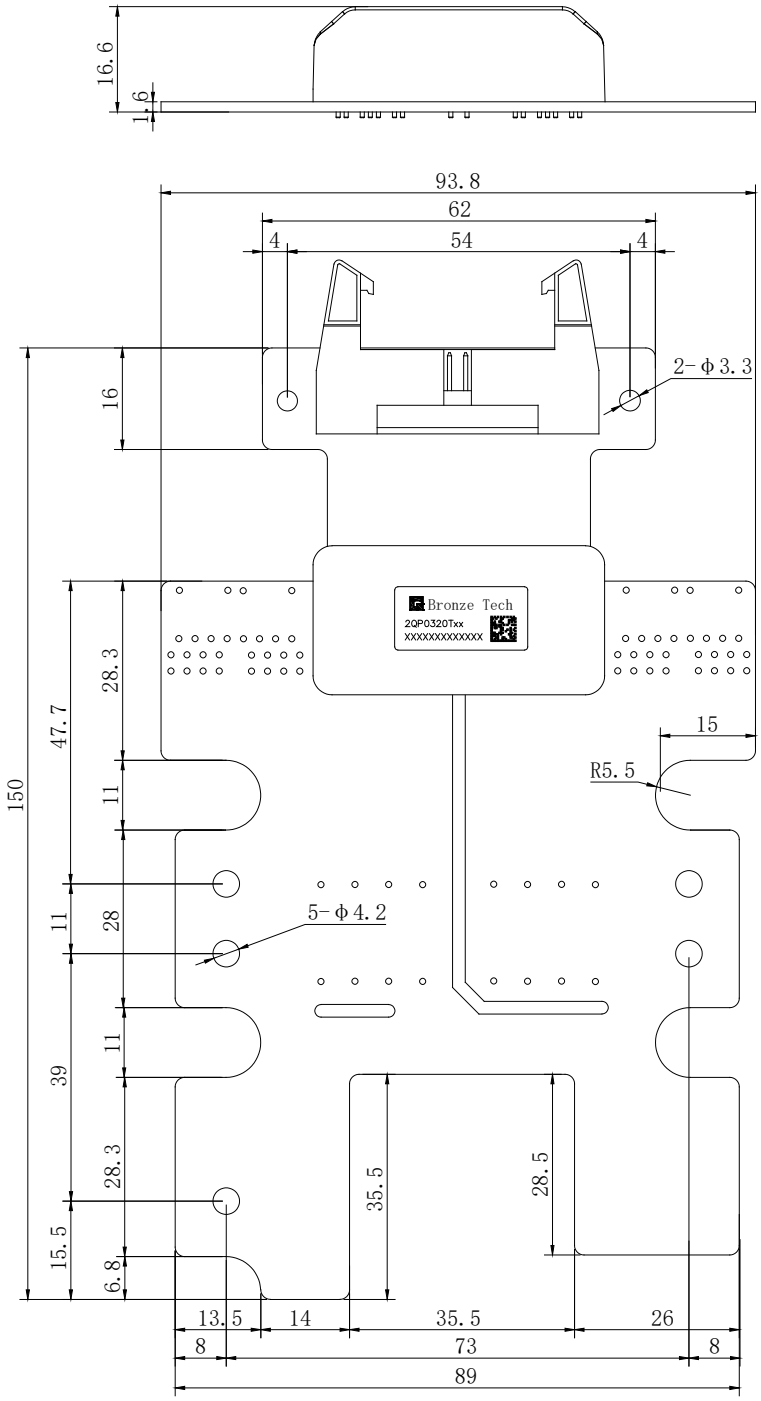


Figure 21. Mechanical drawing of 2QP0320Txx

Note: 1)Legend unit: mm.
2)The margin tolerance conforms with the ISO 2768-1.

Revision History

REVISION	NOTES	DATE
V1.0	Initial release	27-Sep-2023
V1.1	Figures and description updated	04-Nov-2023
V1.2	Active Clamping updated	20-Feb-2024

Precautions

- All operations on the IGBT module and driver shall conform with the electrostatic-sensitive device (ESD) protection requirements stipulated in IEC 60747-1/IX or EN100015.
- To protect ESDs, IGBT module and driver operation, including the operation sites and tools, must conform with these standards.

The IGBT and driver may be damaged due to negligence in ESD protection.

- Before powering on the driver, make sure that the driver and control board are connected correctly, without empty connection, false connection, or false soldering.
- After the driver is installed, its surface voltage to the ground may exceed the safety voltage. Therefore, do not touch it with bare hands.

Operations may involve life hazards. Be sure to follow the corresponding safety protocols !

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